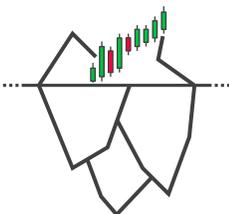


2. NISQ Hardware

Dr. Stefano Gogioso



UNIVERSITY OF
OXFORD



HASHBERG

The NISQ Era

NISQ = Noisy Intermediate-Scale Quantum

- Noisy: high error rate in computations
- Intermediate-scale: few 100s of qubits

Coherence times: Relaxation and Dephasing

Details

27

Qubits

128

QV

1.8K

CLOPS

Status: ● Online

Total pending jobs: 95 jobs

Processor type ⓘ: Falcon r5.1

Version: 1.6.6

Basis gates: CX, ID, RZ, SX, X

Your usage: --

Avg. CNOT Error: 8.373e-2

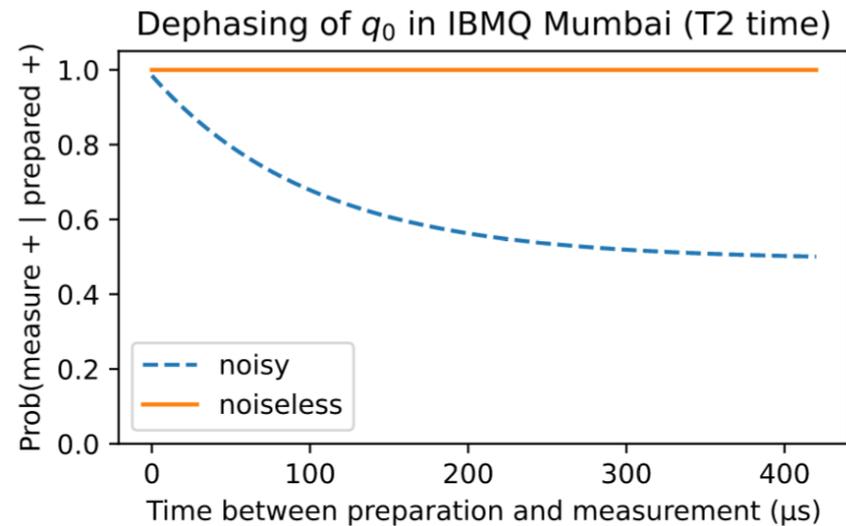
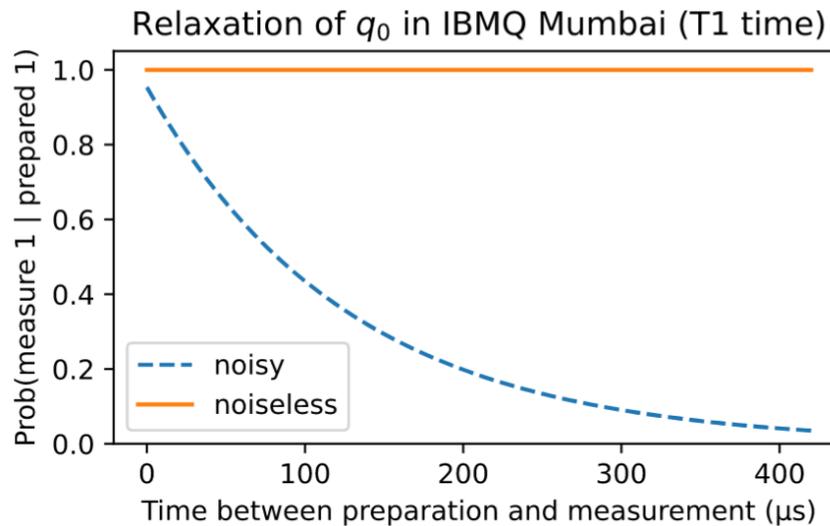
Avg. Readout Error: 3.261e-2

Avg. T1: 127.32 us

Avg. T2: 102.82 us

Providers with access: --

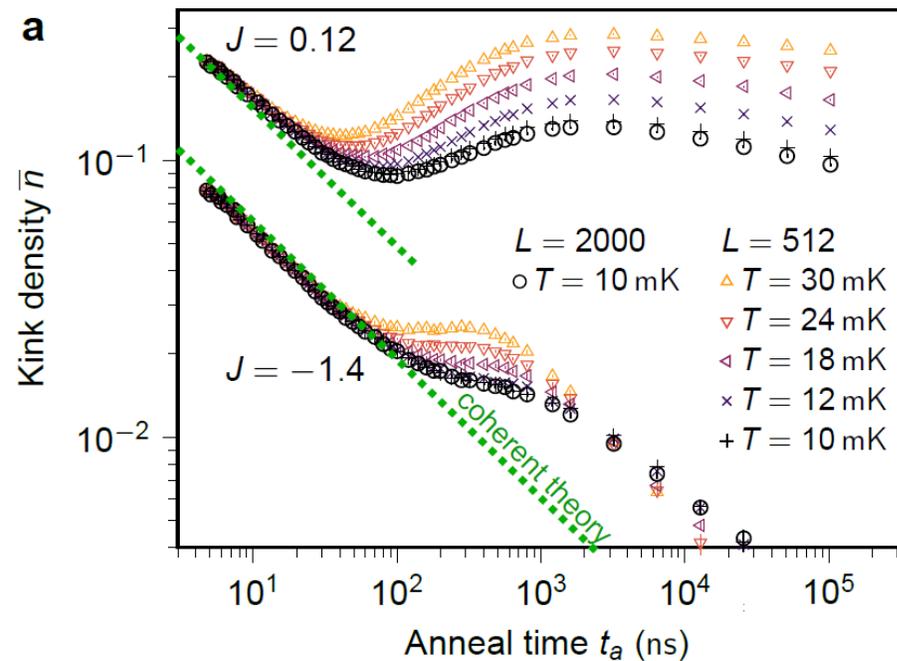
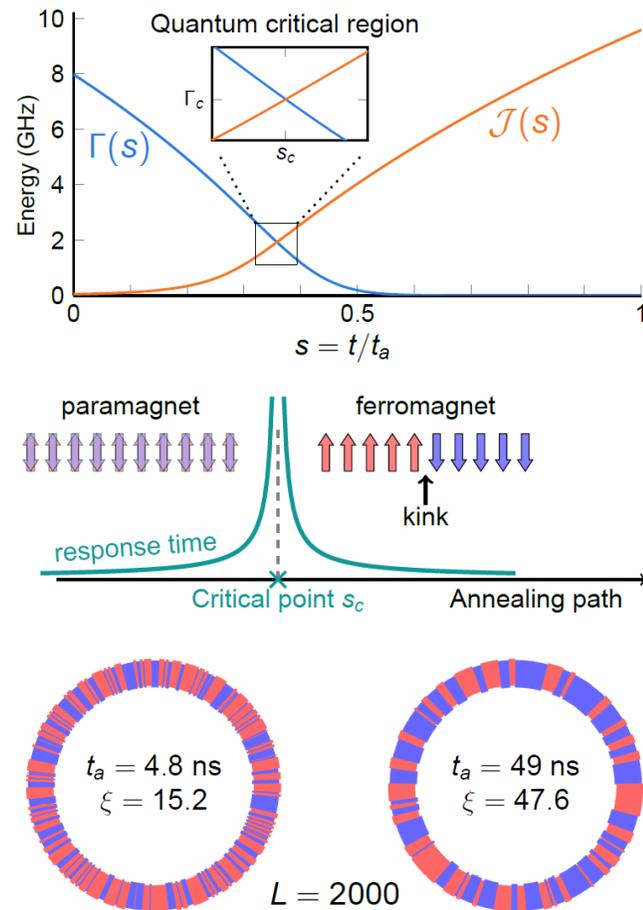
Supports Qiskit Runtime: Yes



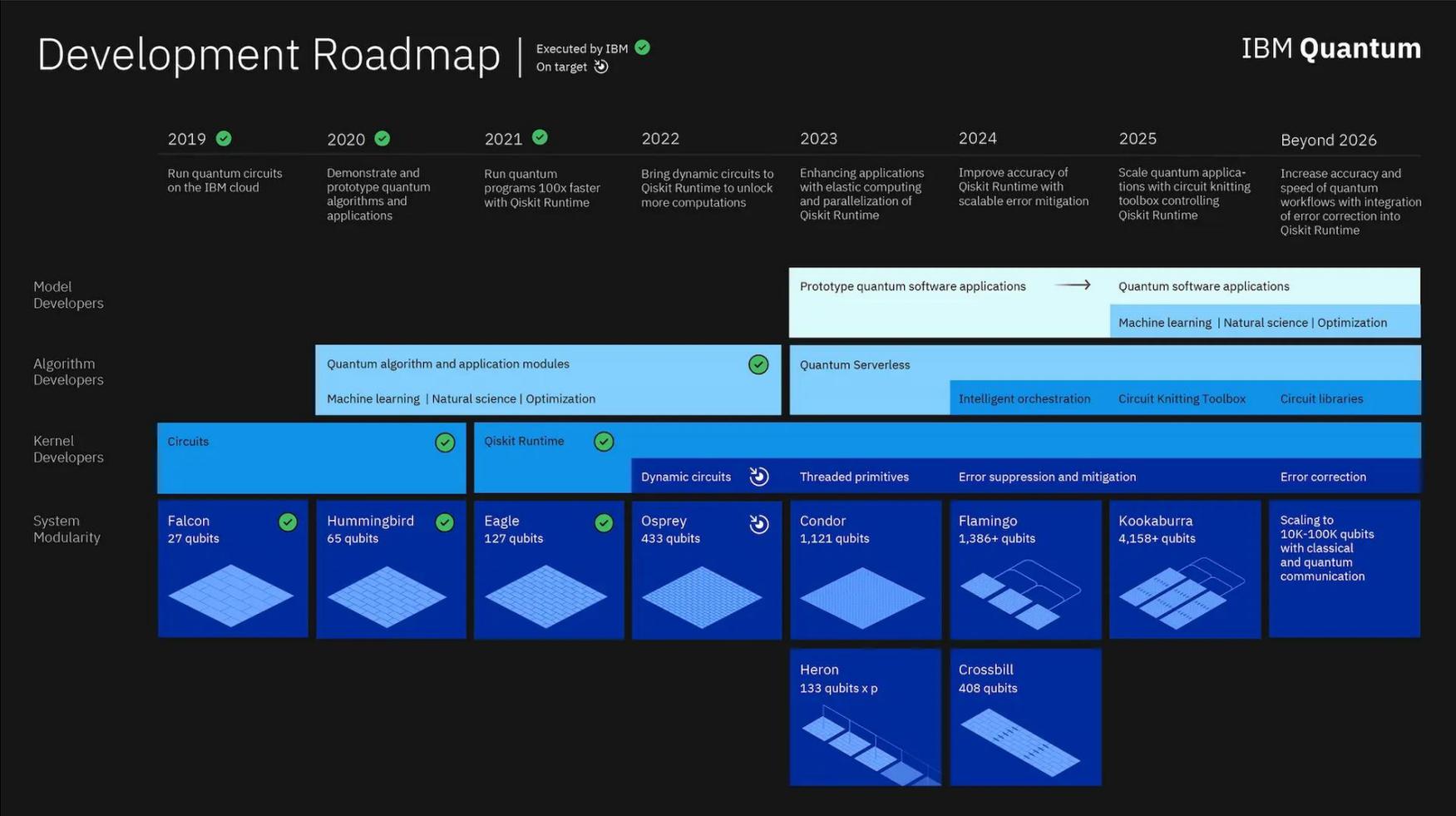
Relaxation and dephasing over $420\mu\text{s}$, the approximate time it takes to execute a circuit with 1000 sequential CX gates.

A 2022 paper by D-Wave, benchmarking the coherence times for their superconducting qubits by measuring the density of “kinks” that form in the (anti-)ferromagnetic regime as a function of the annealing time.

<https://arxiv.org/abs/2202.05847>

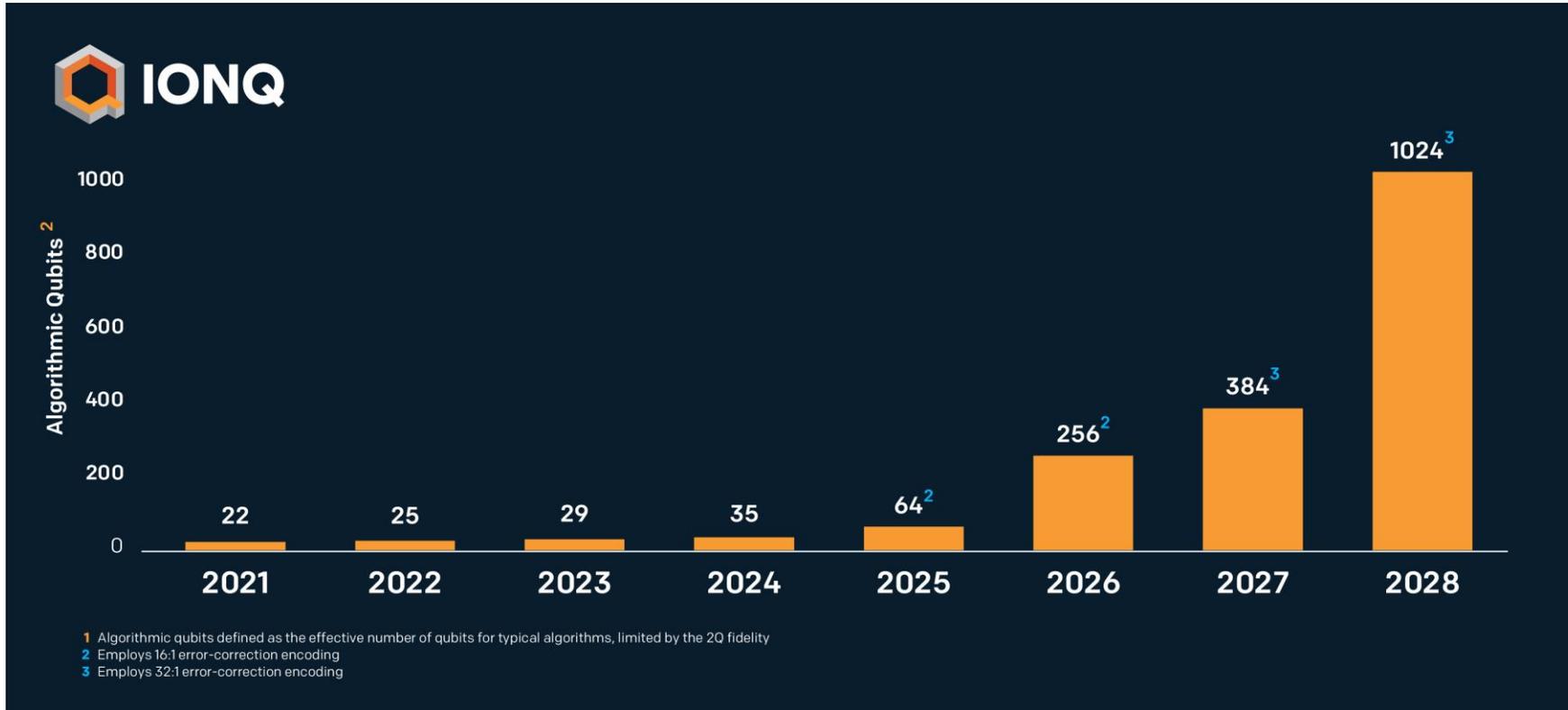


IBM Quantum Roadmap



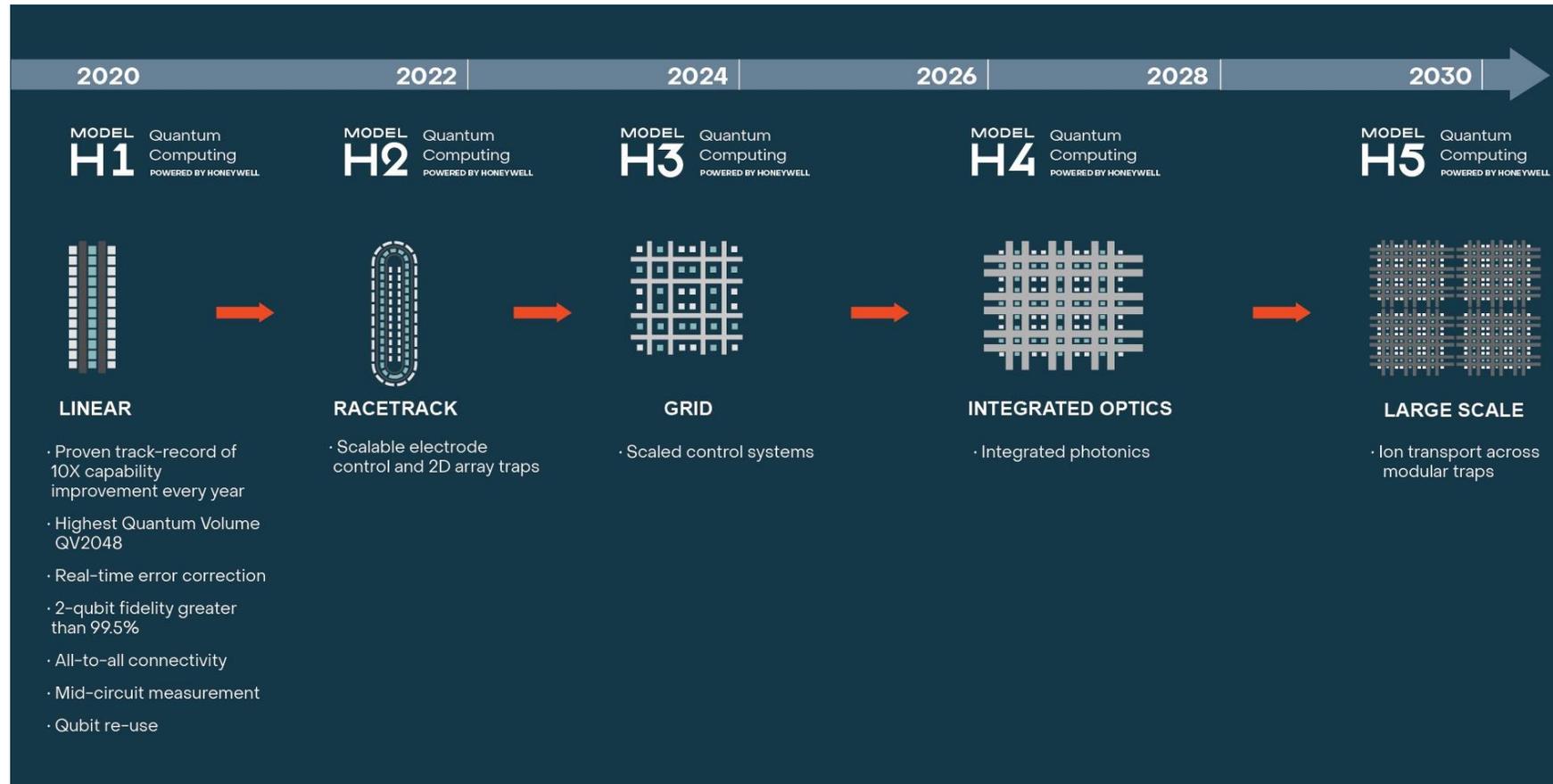
<https://research.ibm.com/blog/ibm-quantum-roadmap-2025>

IonQ Quantum Roadmap

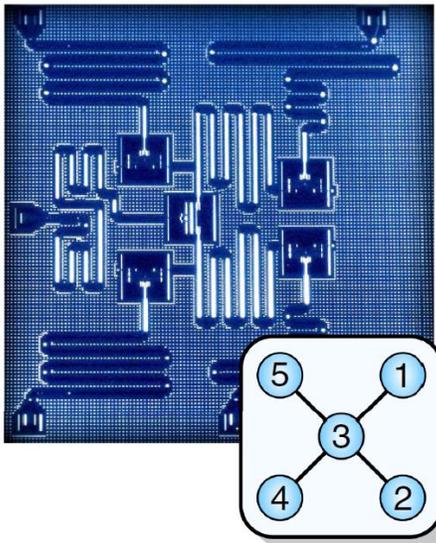


<https://ionq.com/posts/december-09-2020-scaling-quantum-computer-roadmap>

Quantinuum Roadmap



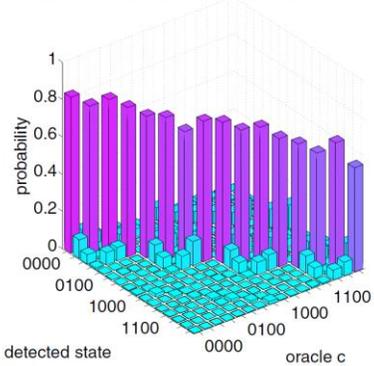
<https://www.quantinuum.com/products/h1>



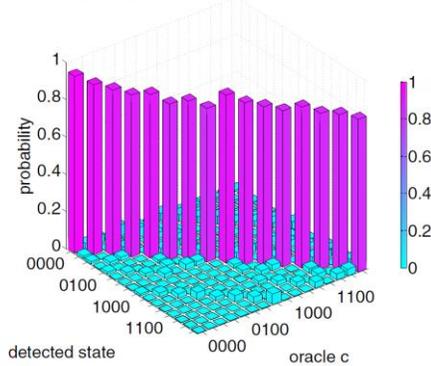
A 2017 paper comparing the noise of 5-qubit superconducting vs ion-trap architectures on some small circuits of interest.

<https://arxiv.org/abs/1702.01852>

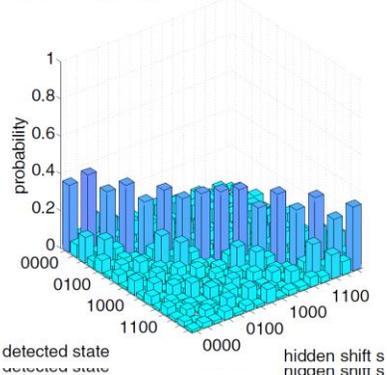
A1 Bernstein-Vazirani: Superconductor



B1 Bernstein-Vazirani: Ion Trap



A2 Hidden shift: Superconductor



B2 Hidden shift: Ion Trap

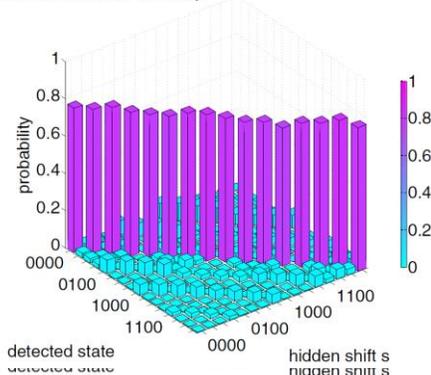
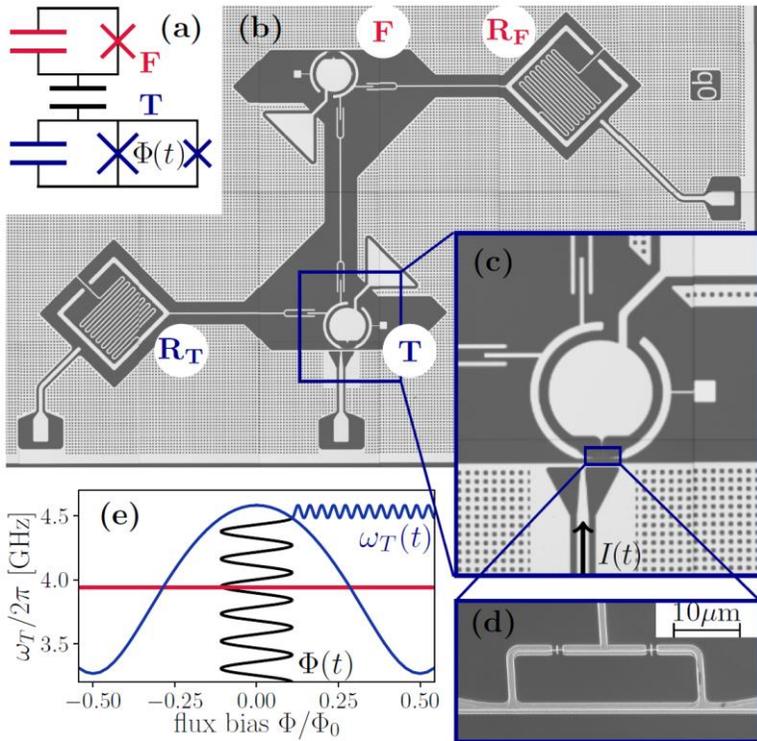
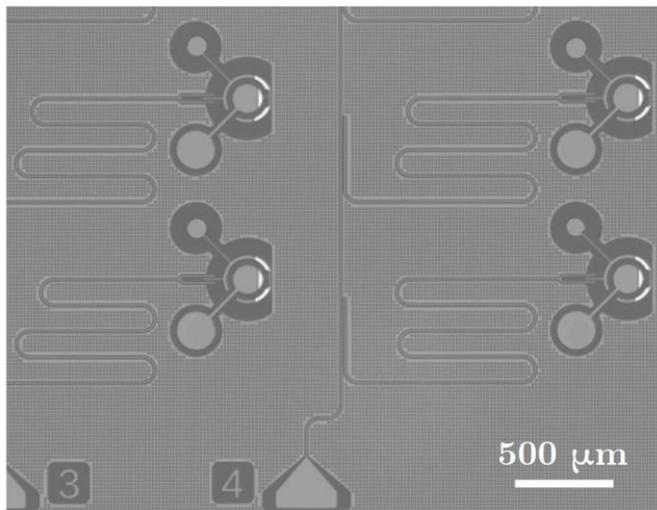


Table 1. Single- and 2-qubit gate counts for the circuits on the superconducting (star-shaped) and the ion-trap (fully connected) system after mapping to the respective hardware using the respective gate libraries

Connectivity	Star		LNN		Full	
Hardware	Superconductor		Superconductor		Ion Trap	
Gate type	1-qubit	2-qubit	1-qubit	2-qubit	1-qubit	2-qubit
Margolus	20	3	20	3	11	3
Toffoli	17	10	9	10	9	5
Bernstein-Vazirani	10	0-4	10	0-10	14-26	0-4
Hidden shift	28-34	10	20-26	4	42-50	4
QFT-3	42	19	11	7	8	3
QFT-5	*	*	35	28	22	10



Above: 2 qubits (2016-06).
Below: 4 qubits (2019-01).



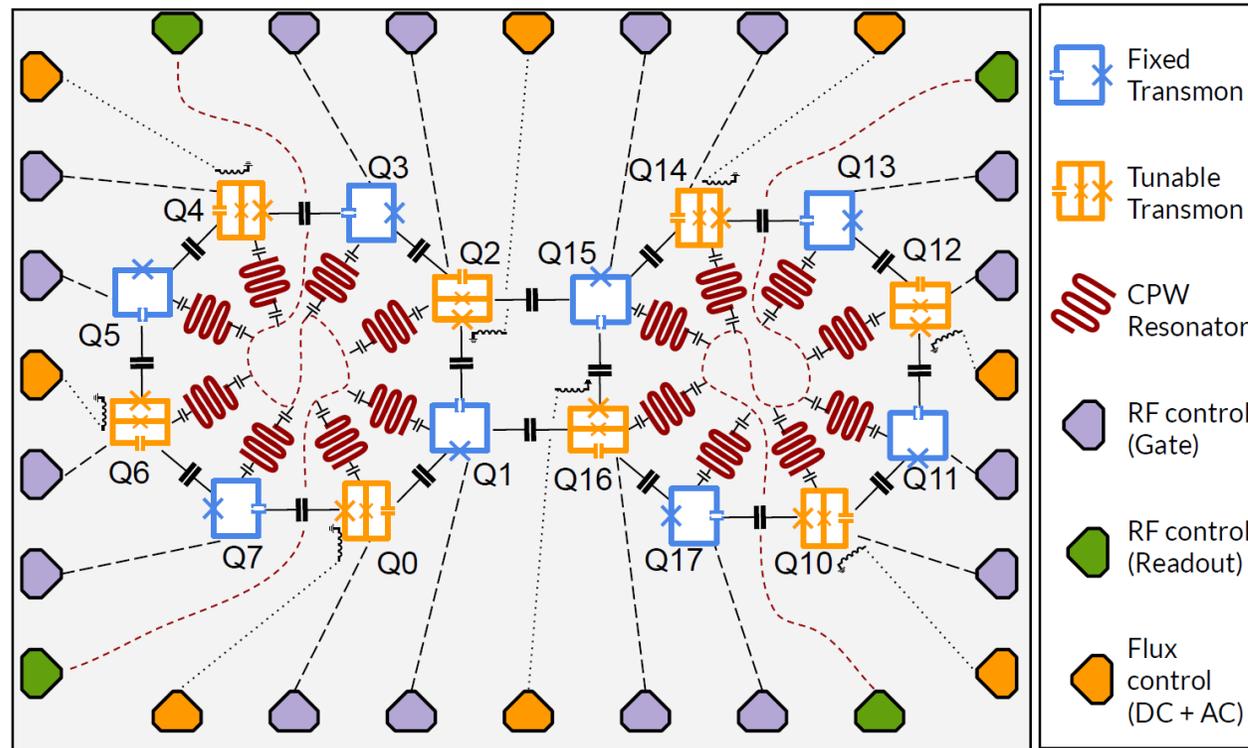
Three papers showing the evolution of Rigetti hardware in 2017-2019:

<https://arxiv.org/abs/1706.06562>

<https://arxiv.org/abs/1901.08042>

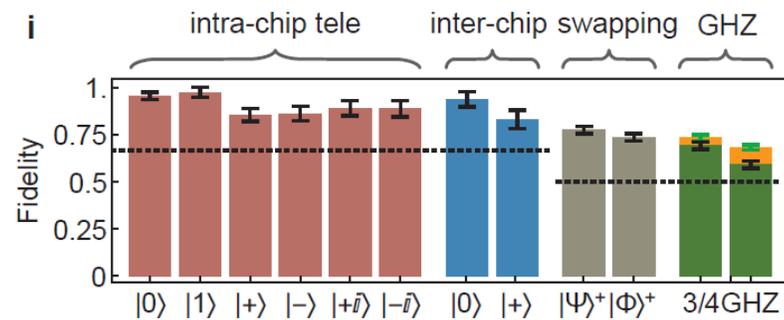
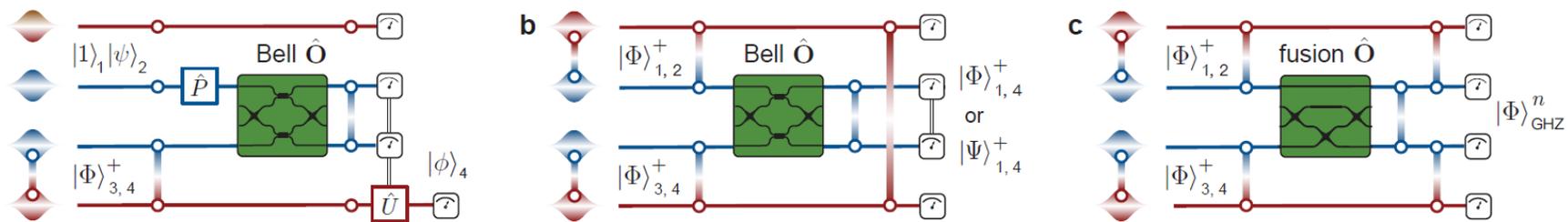
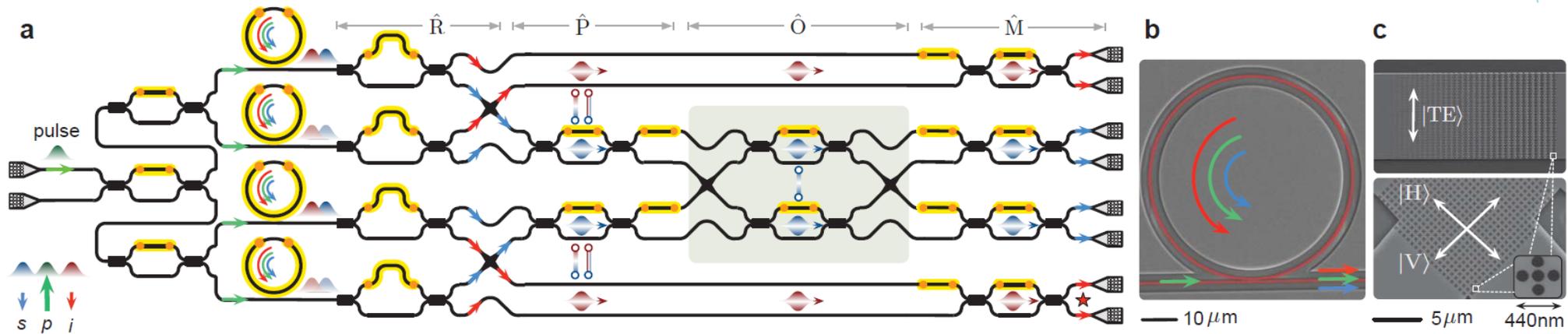
<https://arxiv.org/abs/1908.11856>

Below: 16 qubits (2019-08)



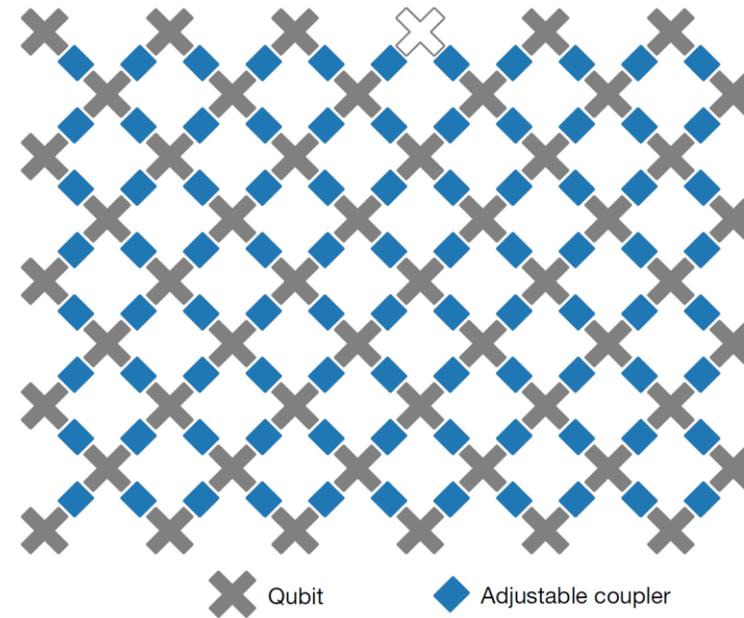
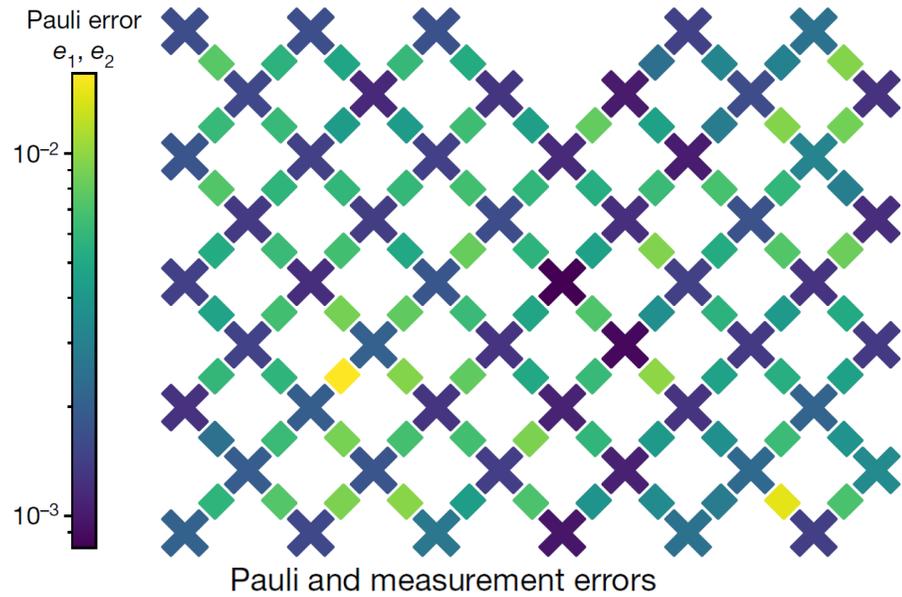
A paper about on-chip quantum optics in 2019 (4 qubits).

<https://arxiv.org/abs/1911.07839>

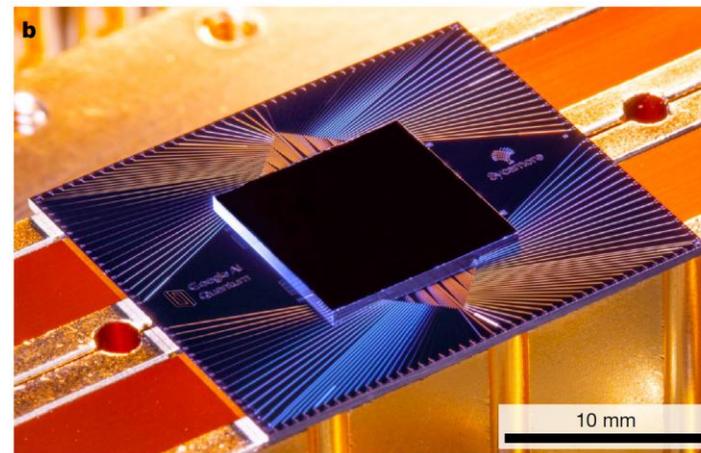


The 2019 Google “quantum supremacy” paper.

<https://www.nature.com/articles/s41586-019-1666-5>

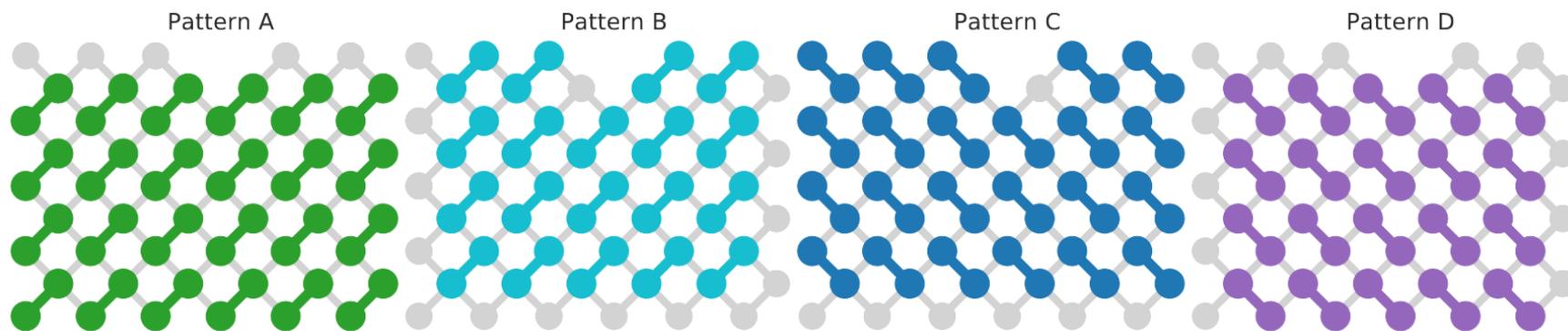
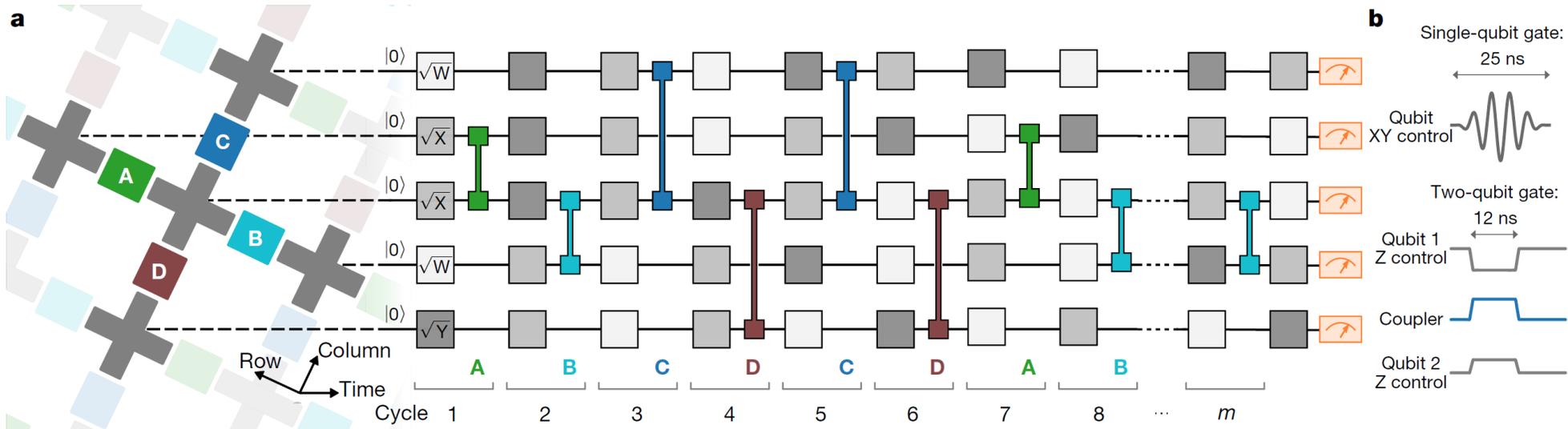


Average error	Isolated	Simultaneous
Single-qubit (e_1)	0.15%	0.16%
Two-qubit (e_2)	0.36%	0.62%
Two-qubit, cycle (e_{2c})	0.65%	0.93%
Readout (e_r)	3.1%	3.8%



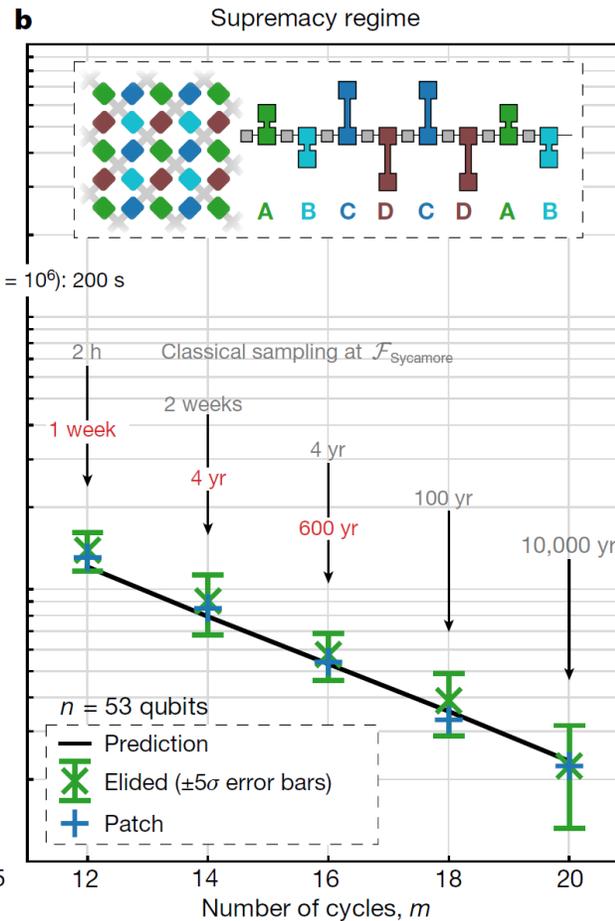
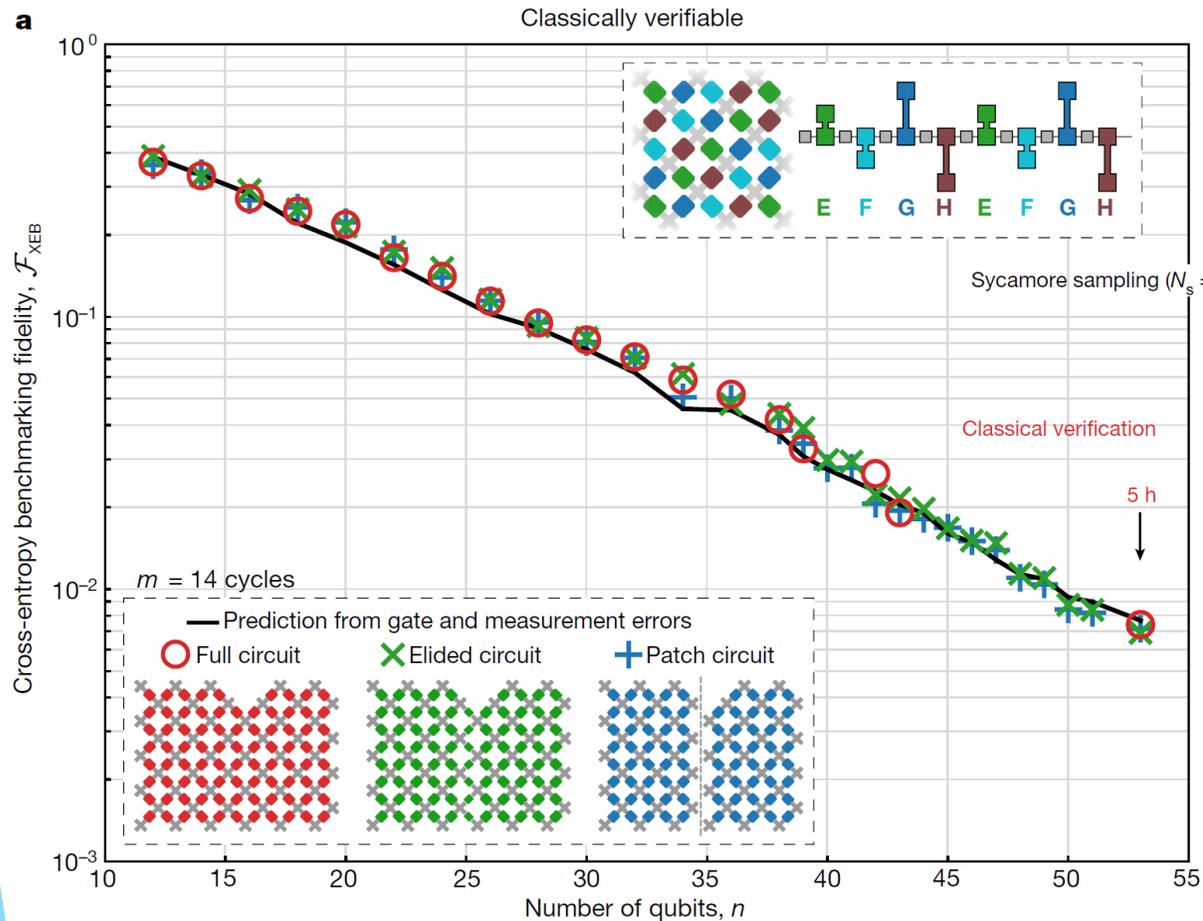
The 2019 Google “quantum supremacy” paper.

<https://www.nature.com/articles/s41586-019-1666-5>

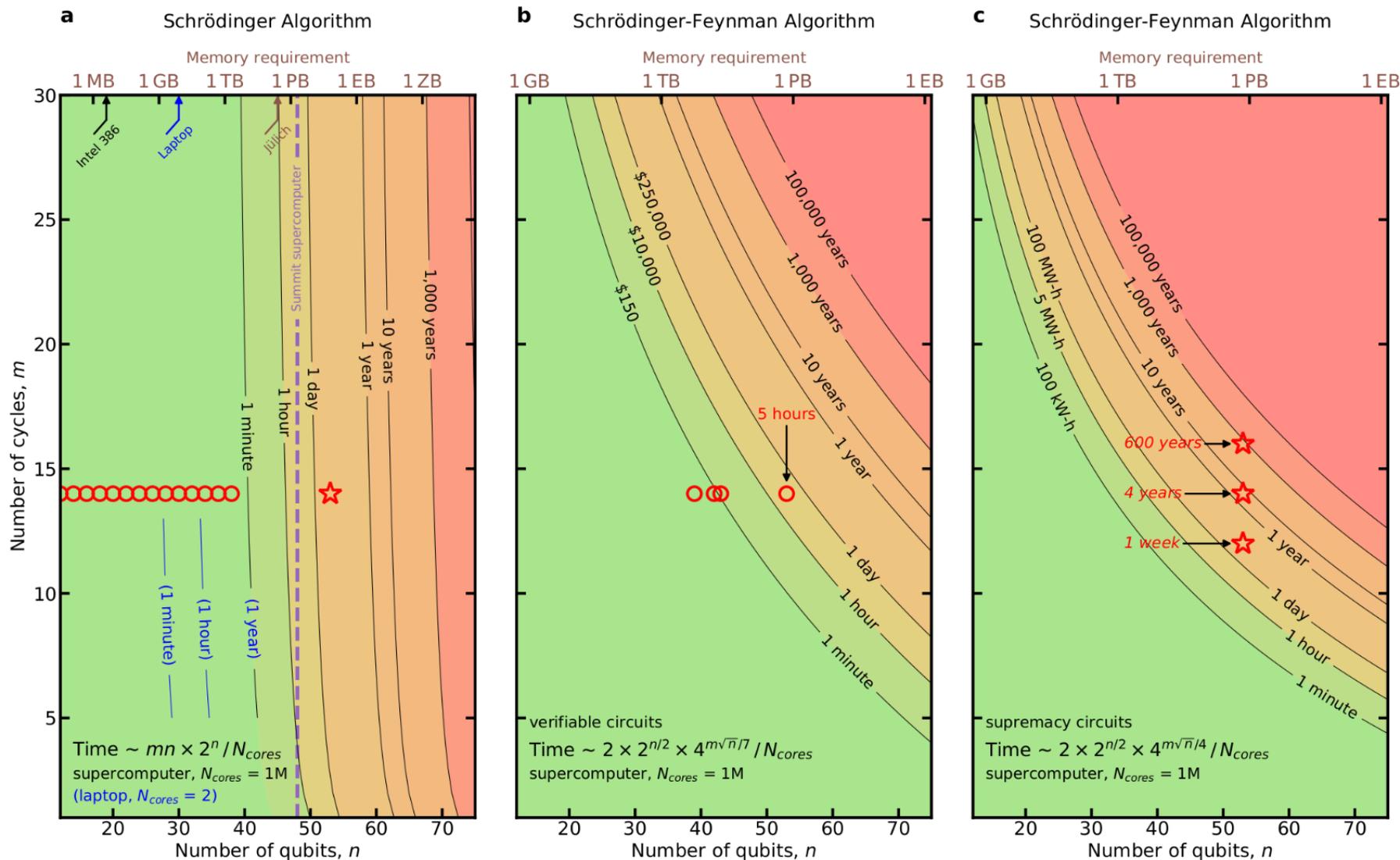


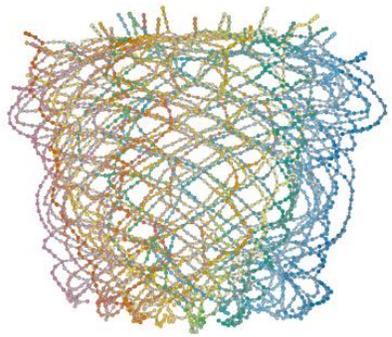
The 2019 Google “quantum supremacy” paper.

<https://www.nature.com/articles/s41586-019-1666-5>

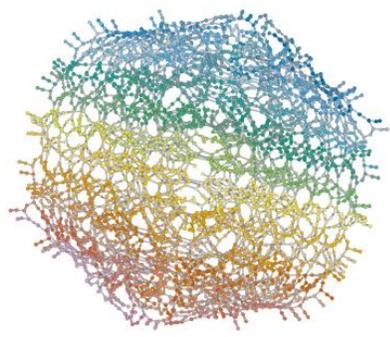


The 2019 Google “quantum supremacy” paper claims that it would take 10k years to simulate their 53-qubits 20-cycle circuits on a supercomputer.

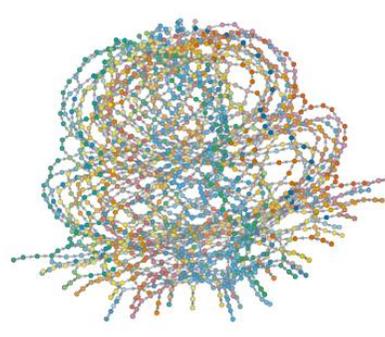




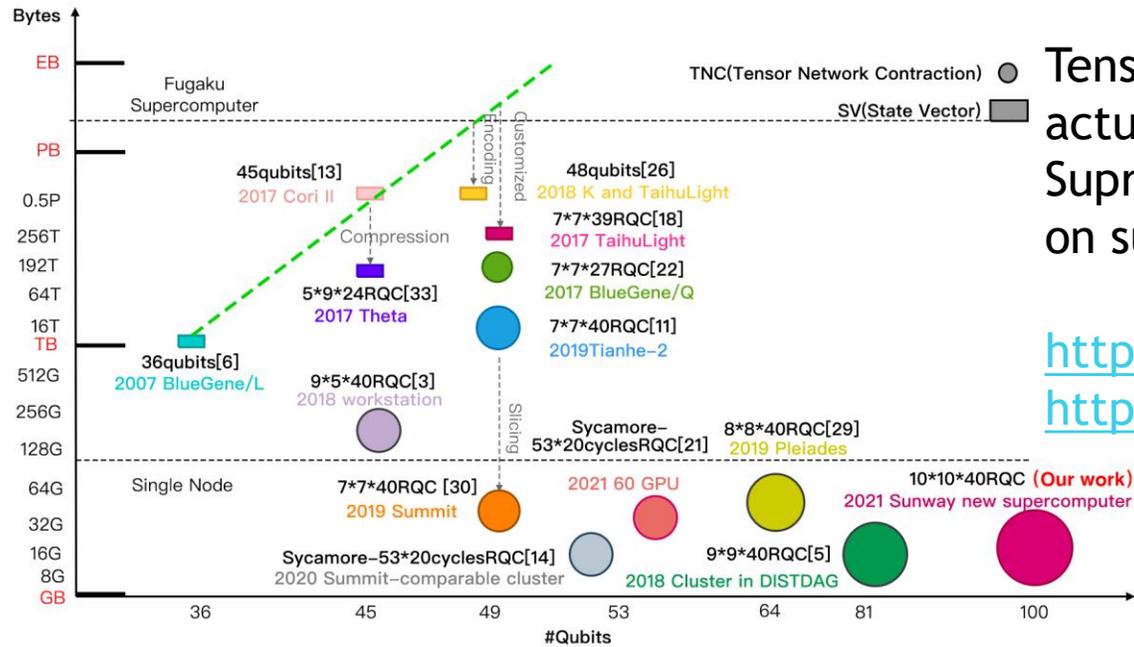
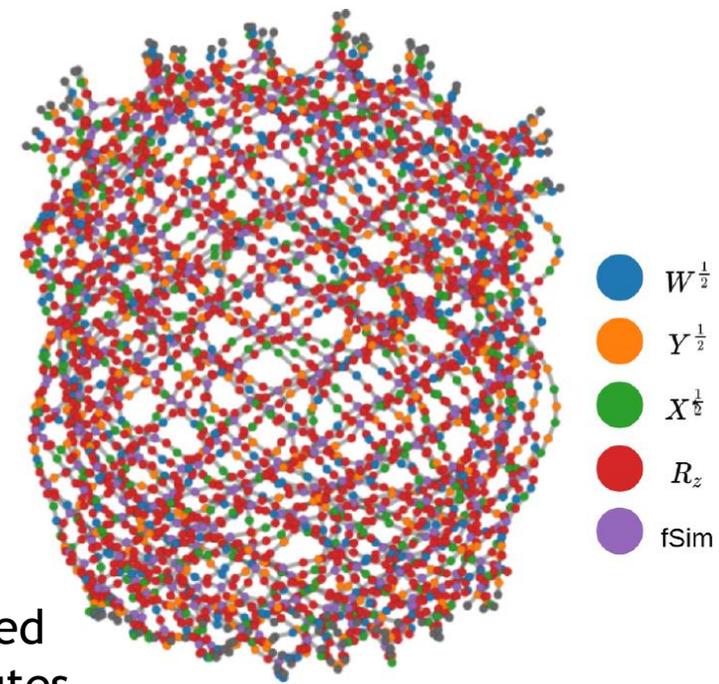
(a) Sycamore



(b) 10x10x(1+40+1)

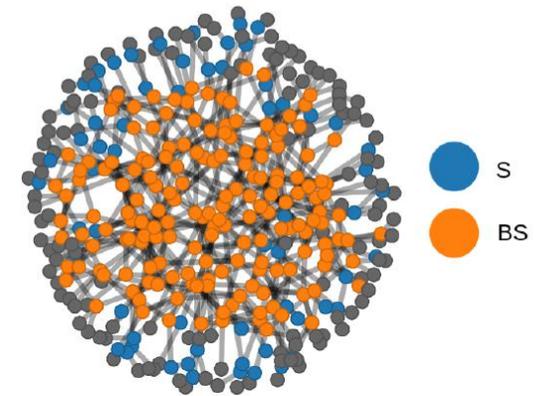


(c) Zuchongzhi



Tensor contraction techniques actually allow the Quantum Supremacy circuits to be simulated on supercomputers in a few minutes.

<https://arxiv.org/abs/2107.09793>
<https://arxiv.org/abs/2110.14502>



Time needed to sample Sycamore

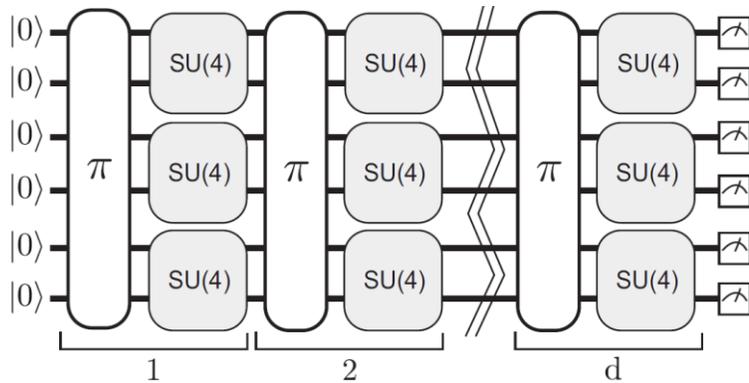
our simulation	304 seconds
physical Sycamore [1]	200 seconds
Summit[1]	10,000 years
Summit[25]	2.55 days (estimated)
Ali_Cloud[14]	19.3 days (estimated)
60_GPUs(Pan)[23]	5 days

Circuit	Slices	Max Size	Time (s)
Syc-53-m20	2^{25}	2.7×10^8	3.5×10^1
Syc-53-m20	0	9.0×10^{15}	1.6×10^1
GBS-444-m1	4^{14}	6.7×10^7	3.6×10^2
GBS-444-m1	0	4.4×10^{12}	1.7×10^{-1}
GBS-666-m1	0	7.9×10^{28}	2.1×10^{14}

IBM uses a metric known as Quantum Volume (QV) to benchmark their quantum computers.

<https://arxiv.org/abs/1811.12926>

By its definition, the metric appears to grow exponentially: the interesting quantity is $\log_2(QV)$, the size of the largest “square” circuit which generates enough “heavy outputs”.



To define when a model circuit U has been successfully implemented in practice, we use the heavy output generation problem [19]. The ideal output distribution is

$$p_U(x) = |\langle x|U|0\rangle|^2, \quad (2)$$

where $x \in \{0, 1\}^m$ is an observable bit string. Consider the set of output probabilities given by the range of $p_U(x)$ sorted in ascending order $p_0 \leq p_1 \cdots \leq p_{2^m-1}$. The median of the set of probabilities is $p_{\text{med}} = (p_{2^{(m-1)}} + p_{2^{(m-1)}-1})/2$ and the heavy outputs are

$$H_U = \{x \in \{0, 1\}^m \text{ such that } p_U(x) > p_{\text{med}}\}. \quad (3)$$

The heavy output generation problem is to produce a set of output strings such that more than two-thirds are heavy.

Algorithm 1. Check heavy output generation.

```

function ISHEAVY( $m, d; n_c \geq 100, n_s$ )
   $n_h \leftarrow 0$ 
  for  $n_c$  repetitions do
     $U \leftarrow$  random model circuit, width  $m$ , depth  $d$ 
     $H_U \leftarrow$  heavy set of  $U$  from classical simulation
     $U' \leftarrow$  compiled  $U$  for available hardware
    for  $n_s$  repetitions do
       $x \leftarrow$  outcome of executing  $U'$ 
      if  $x \in H_U$  then  $n_h \leftarrow n_h + 1$ 
  return  $\frac{n_h - 2\sqrt{n_h(n_s - n_h/n_c)}}{n_c n_s} > \frac{2}{3}$ 

```

We define the quantum volume V_Q as

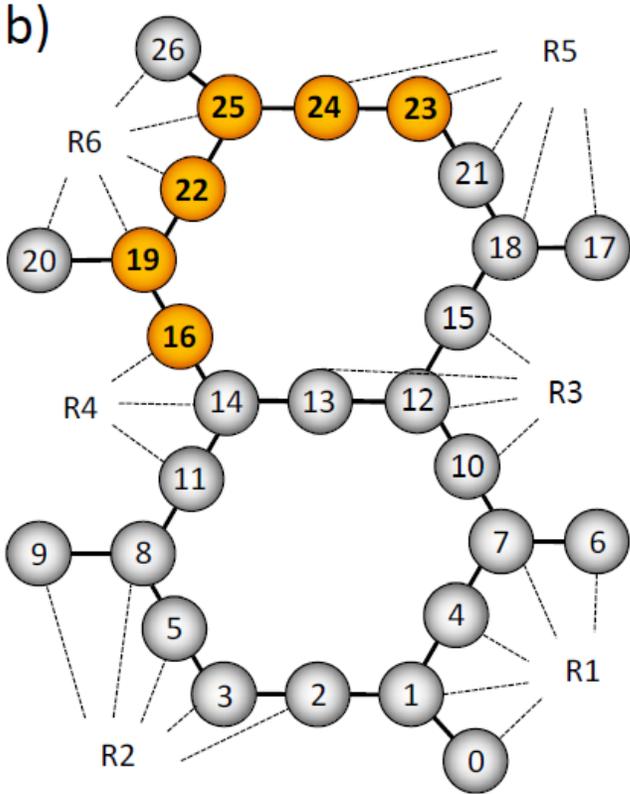
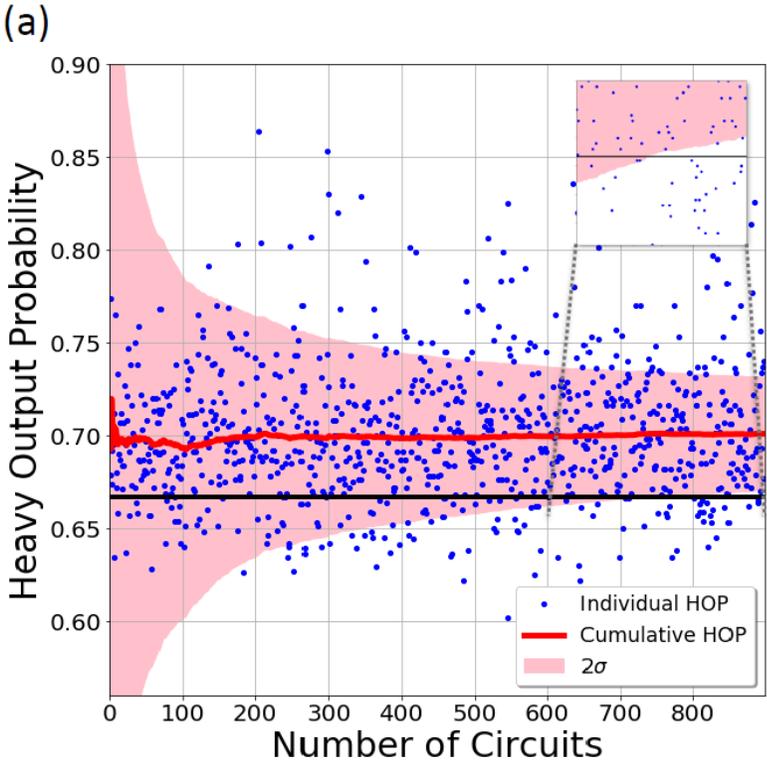
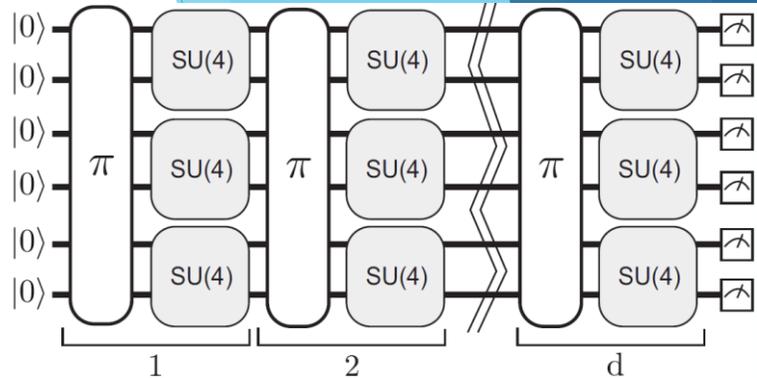
$$\log_2 V_Q = \operatorname{argmax}_m \min(m, d(m))$$

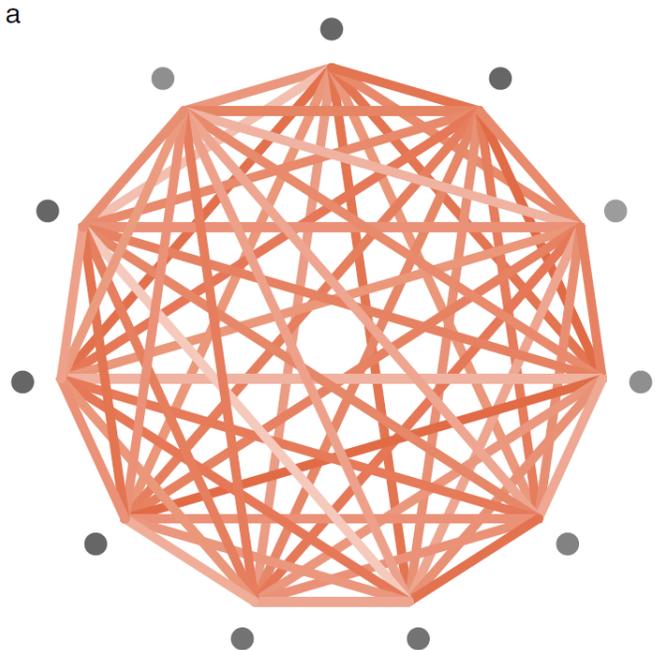
and take this definition going forward.

Name	Qubits	QV
ibmq_montreal	27	128
ibmq_mumbai Exploratory	27	128
ibmq_cairo	27	64
ibmq_auckland Exploratory	27	64
ibmq_toronto	27	32
ibmq_guadalupe	16	32
ibmq_perth	7	32
ibmq_lagos	7	32
ibmq_nairobi	7	32
ibmq_jakarta	7	16
ibmq_manila	5	32
ibmq_bogota	5	32
ibmq_santiago	5	32
ibmq_quito	5	16
ibmq_belem	5	16
ibmq_lima	5	8

A 2020 paper verifying QV 64 (i.e. $HOP > \frac{2}{3}$ on 6 qubits with depth $d = 6$) to a confidence of 2σ for the 27-qubit device IBMQ Montreal (currently at QV 128).

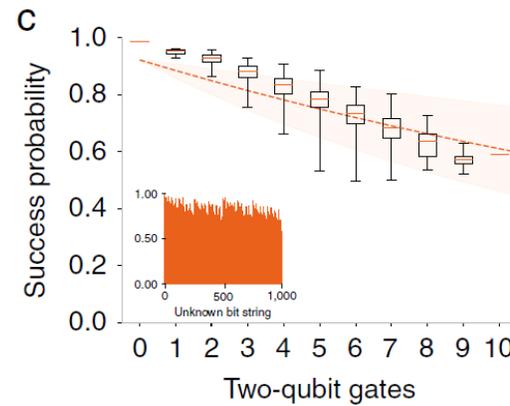
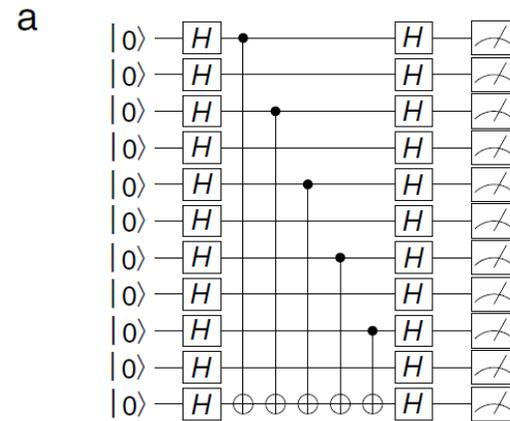
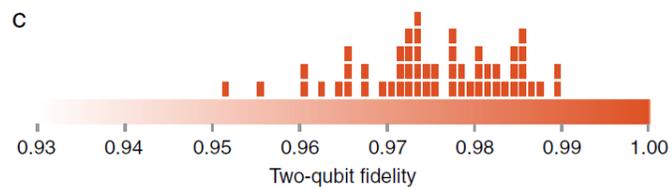
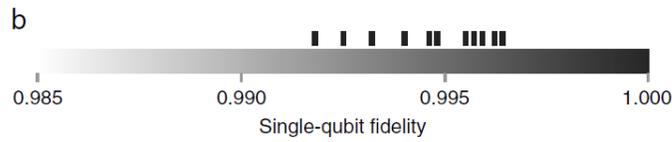
<https://arxiv.org/abs/2008.08571>



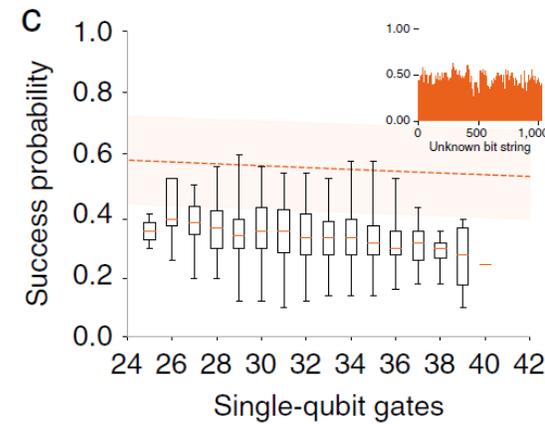
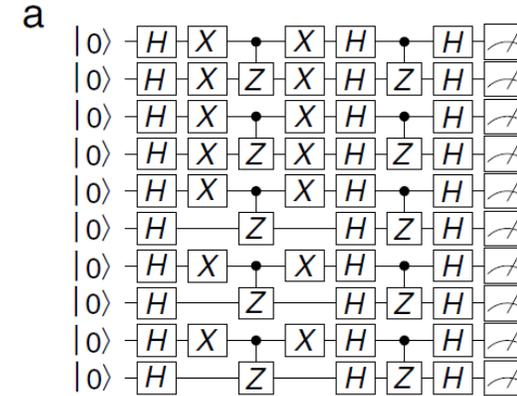


A 2020 IonQ paper benchmarking an 11-qubit ion trap.

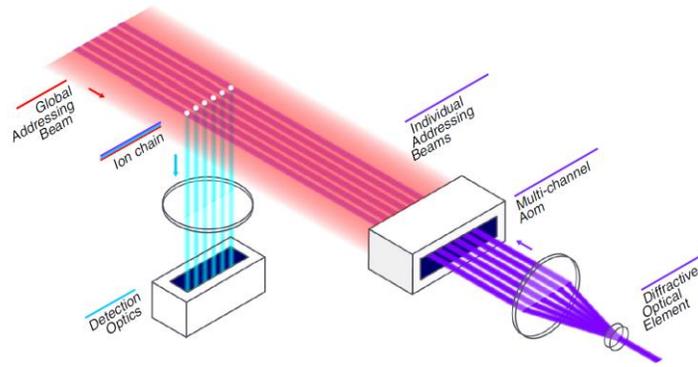
<https://www.nature.com/articles/s41467-019-13534-2>



Bernstein-Vazirani

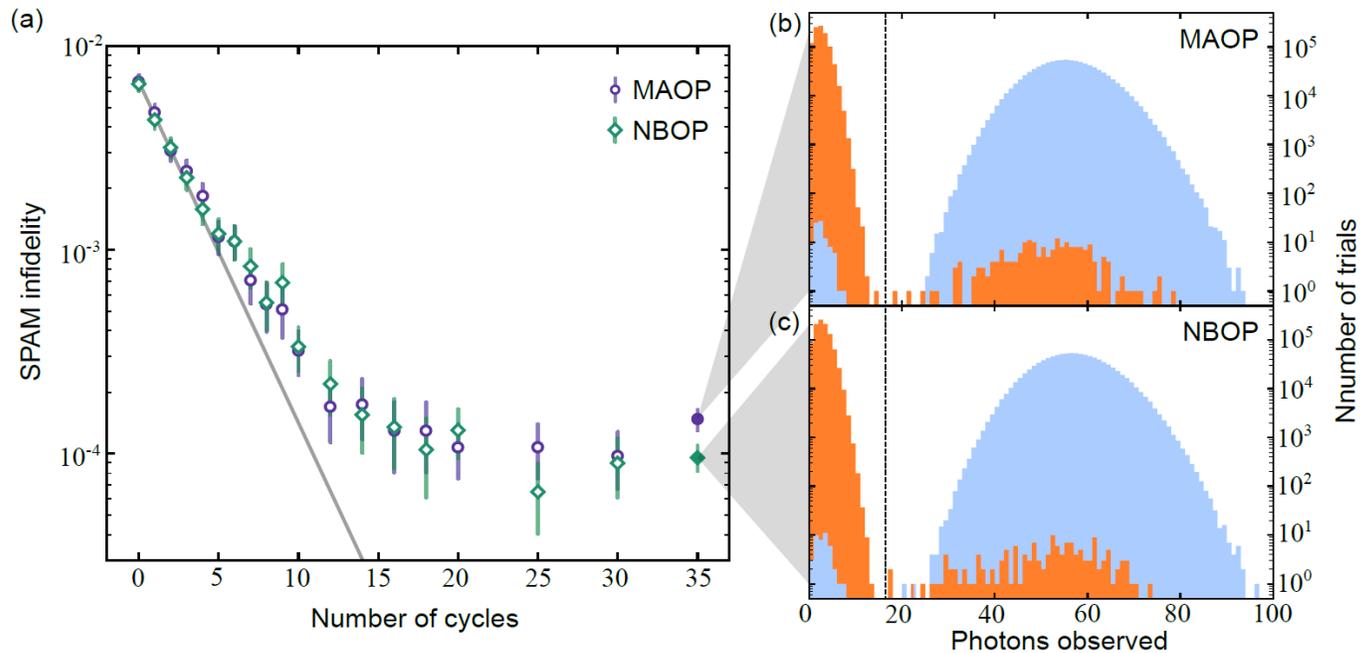


Hidden Shift



A 2022 Quantinuum paper benchmarking State Preparation And Measurement (SPAM) fidelity in their ion trap quantum computers, using two optical pumping techniques (MAOP and NBOP) to reduce state preparation errors to around 0.1%, the approximate threshold for some interesting error correction schemes.

<https://arxiv.org/abs/2203.01920>

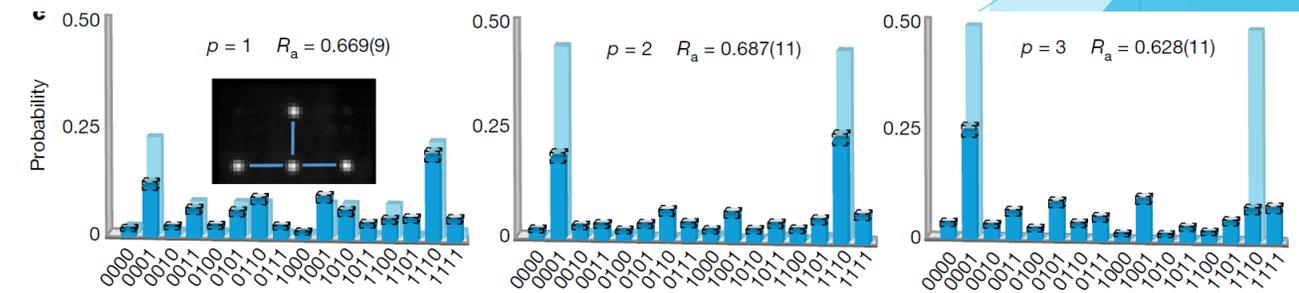
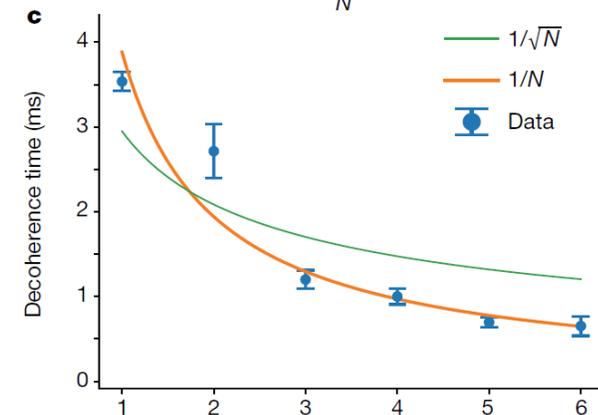
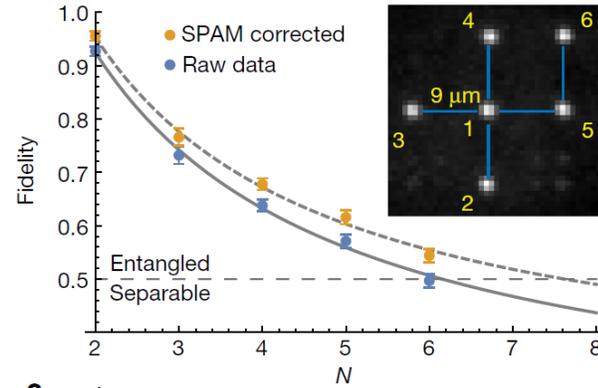
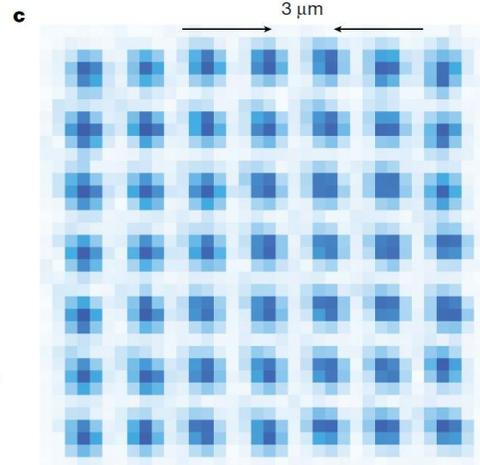
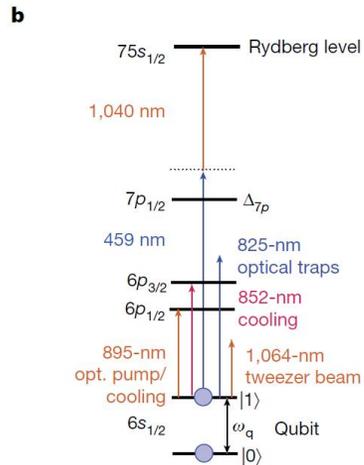
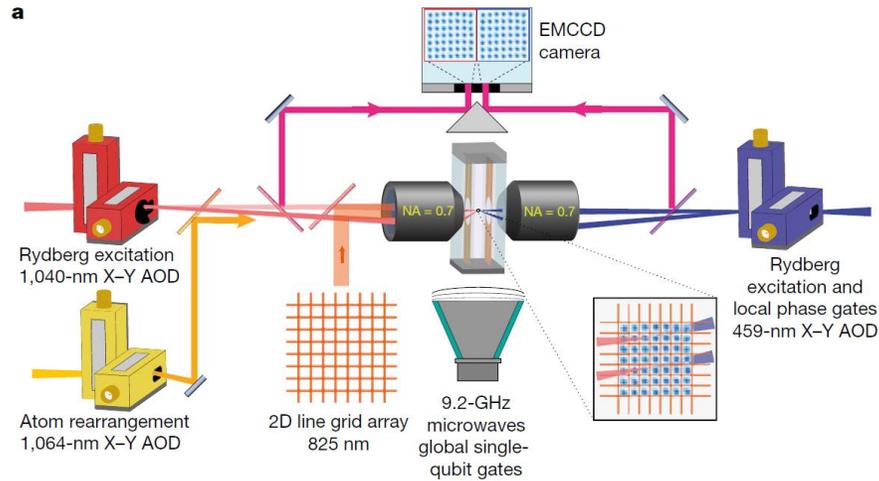


Error Source	Error ($\times 10^{-5}$)	
	$ 0\rangle$ State	$ 1\rangle$ State
$ 0\rangle$ state preparation	<9.1	—
$ 0\rangle \rightarrow 1\rangle$ transfer	—	5.4 ± 0.5
Shelving infidelity	~ 0.1	—
$D_{5/2}$ decay	~ 1.5	—
Correlated errors	4.0	—
Subtotal (measured)	14.7 ± 2.4	4.2 ± 1.3
Total (measured)	9.6 ± 1.4	

On the right: vertical bar is the threshold separating the $|0\rangle$ and $|1\rangle$ states. Histogram of $|0\rangle$ state preparation in orange, histogram of $|1\rangle$ state preparation in blue.

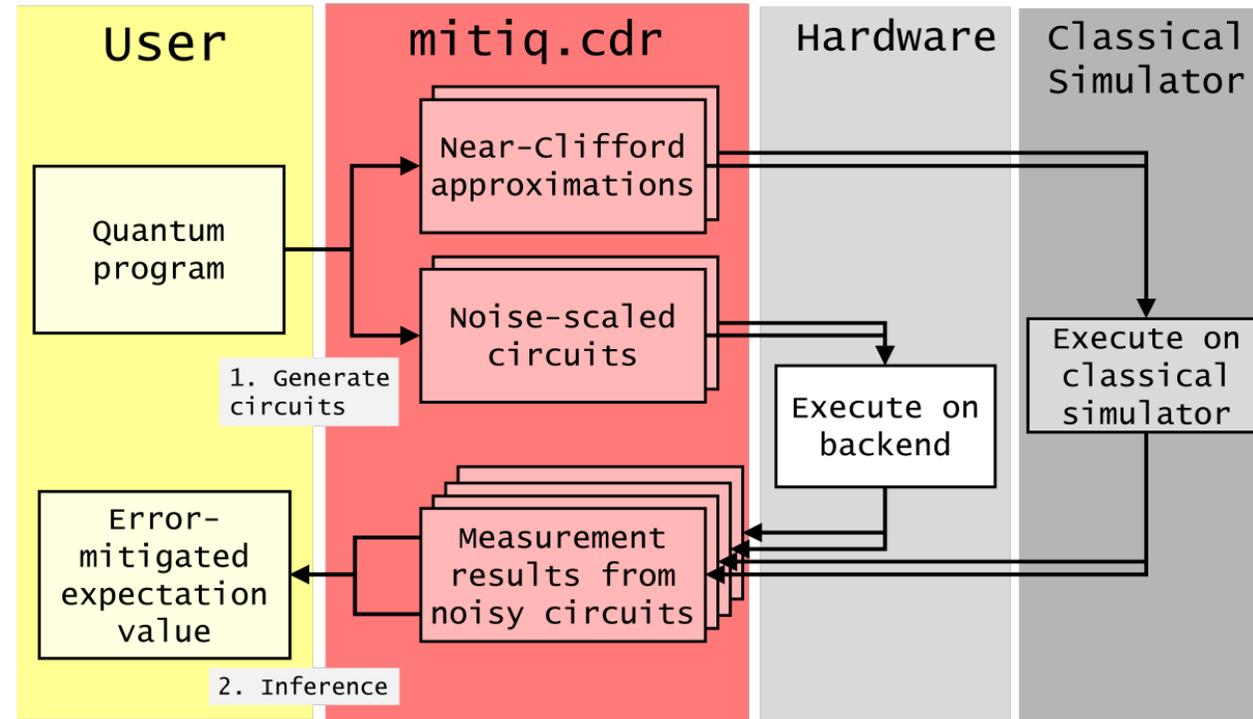
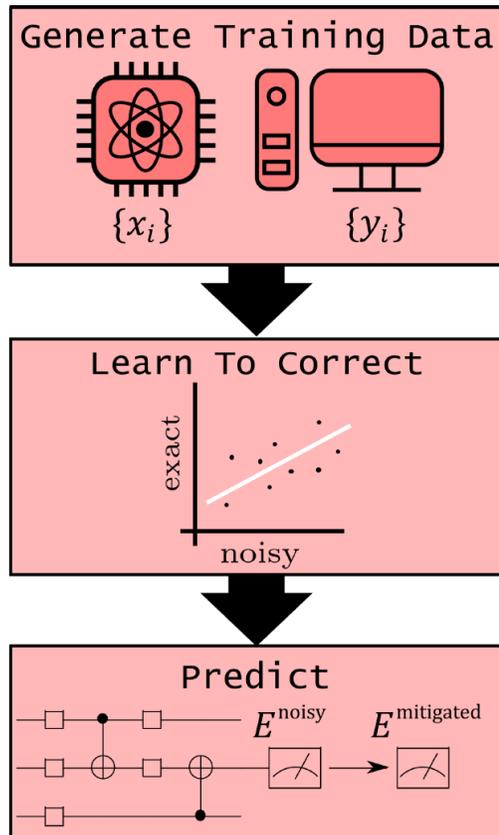
A 2022 paper benchmarking highly entangled GHZ states on 6 qubits in a neutral atom quantum computer.

<https://www.nature.com/articles/s41586-022-04603-6>



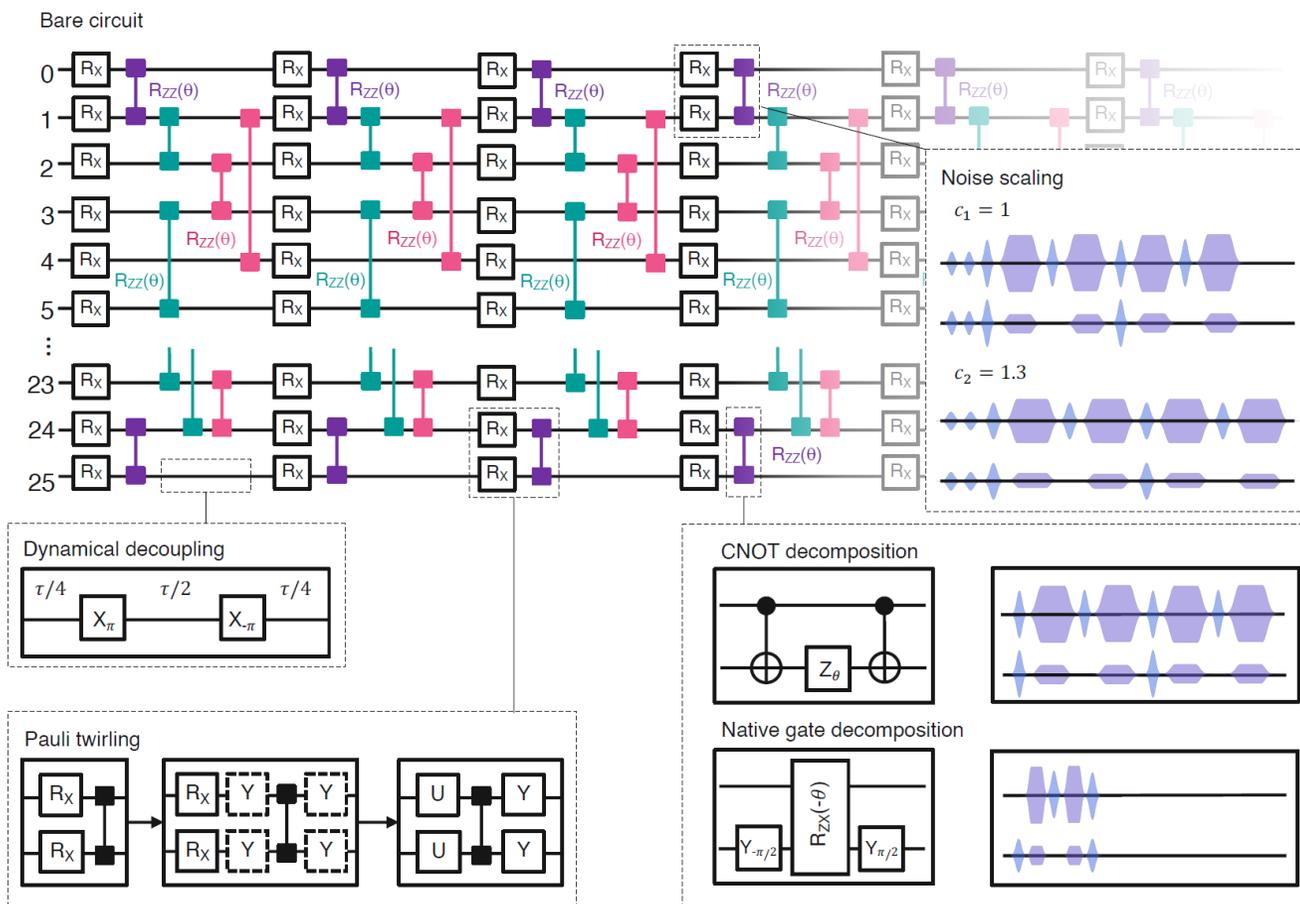
2020 paper introducing an error mitigation library for NISQ computations.

<https://arxiv.org/abs/2009.04417>

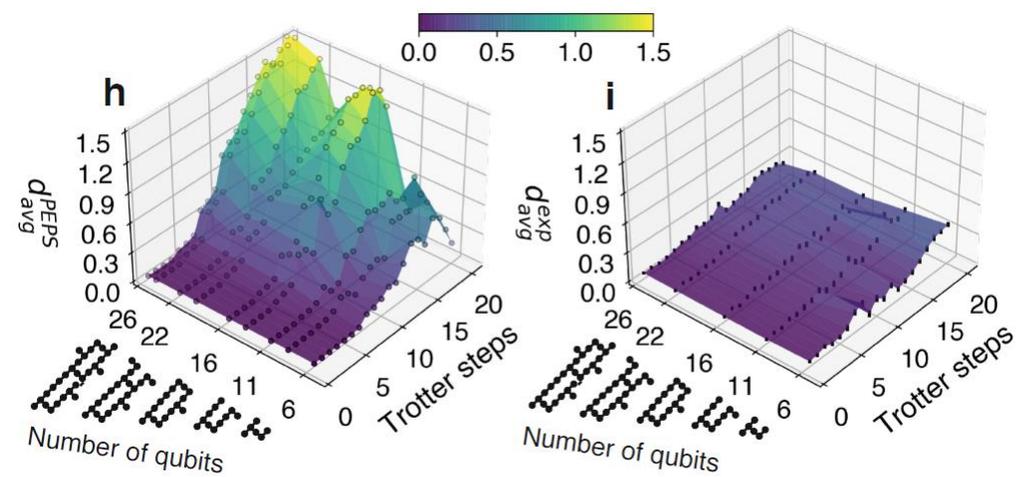


A 2021 error mitigation paper by IBM. Noise scaling is used to extrapolate noise profiles, dynamical decoupling to reduce dephasing, Pauli twirling to average-out coherent errors and native decomposition to reduce the total circuit execution time (and hence the noise).

<https://arxiv.org/abs/2108.09197>

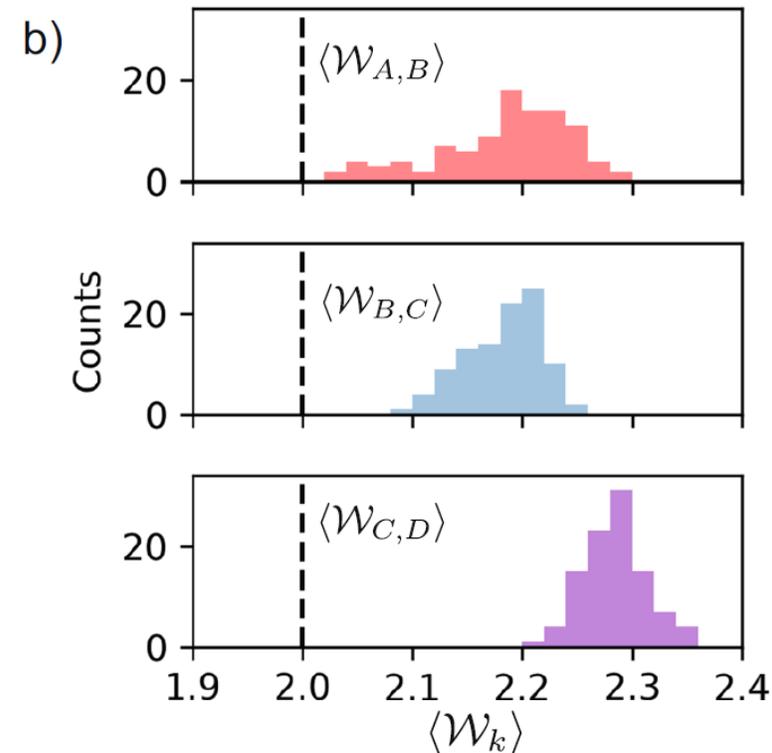
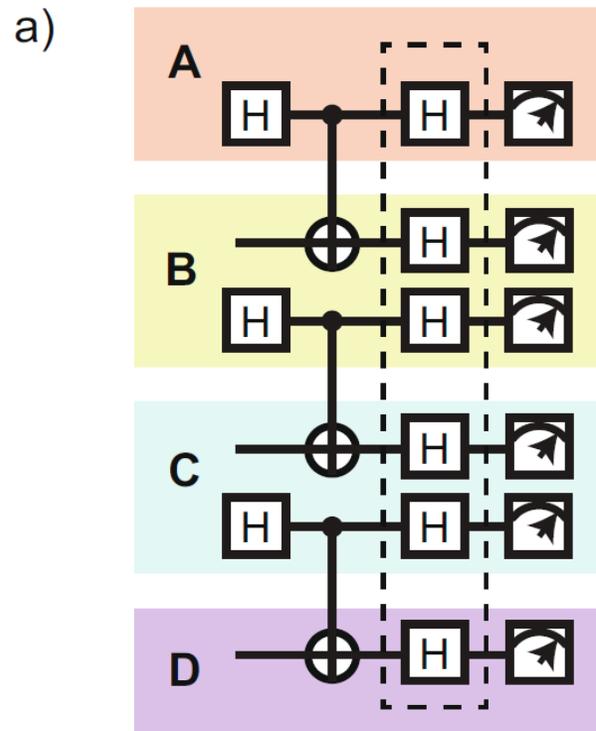
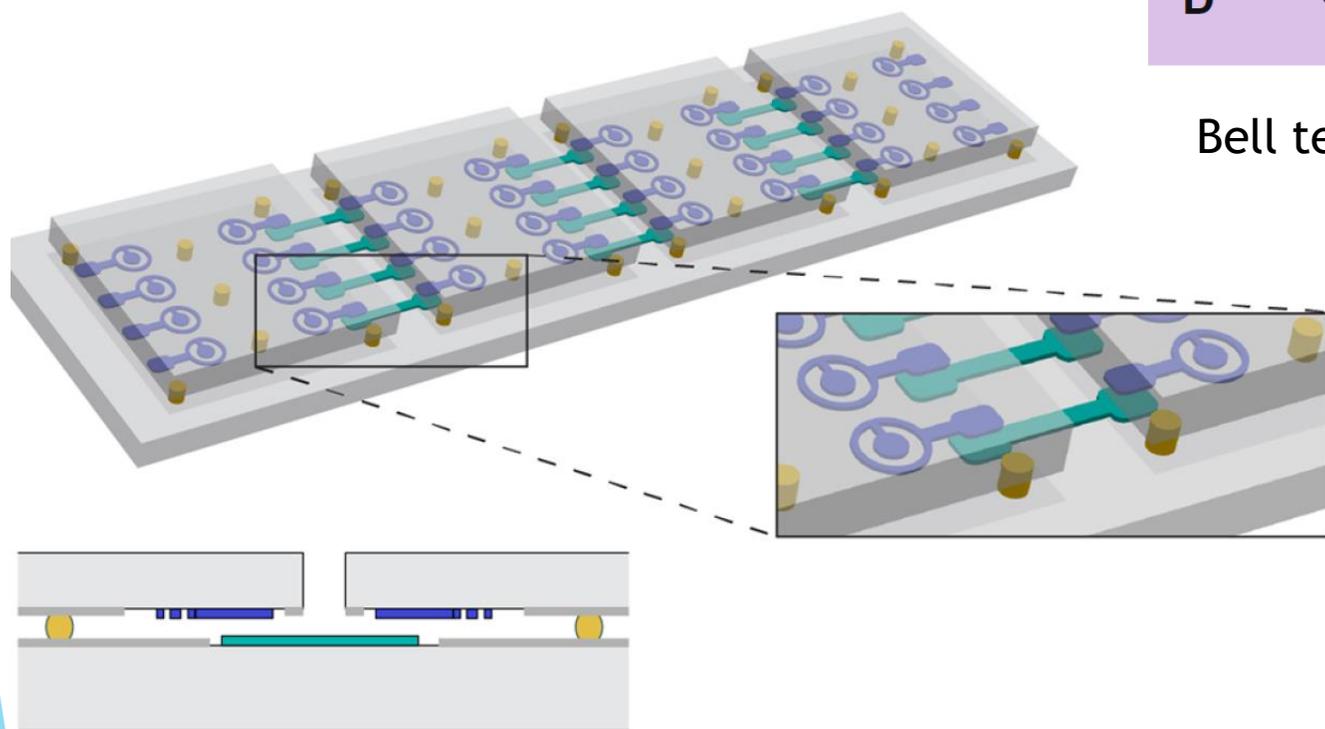


Below: simulation error for quench dynamics of 2D Ising spin lattices, as a function of size and number of simulation steps. Standard technique (left) versus error mitigation (right).



A 2021 Rigetti paper benchmarking entanglement in a multi-chip quantum processor.

<https://arxiv.org/abs/2102.13293>



Bell test across 4 chips: W above 2 \Rightarrow entanglement.

IBM proposals for multi-chip quantum processors

<https://research.ibm.com/blog/ibm-quantum-roadmap-2025>

